

## **EMI CANCELLATION METHOD AND SYSTEM**

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### **CROSS REFERENCE TO RELATED APPLICATION**

[0001] This application is based on Korea Patent Application No. 2002-66134 filed on October 29, 2002 in the Korean Intellectual Property Office, the content of which is incorporated in its entirety herein by this reference.

### **BACKGROUND OF THE INVENTION**

#### **(a) Field of the Invention**

[0002] The present invention relates to an electromagnetic interference (EMI) cancellation method and system.

#### **(b) Description of the Related Art**

[0003] The term electromagnetic interference means any electromagnetic disturbance that interrupts, degrades, or limits the effective performance of electrical equipment or systems. In particular, high frequency electric noise emitted from an electric device via small integrated chips imparts a negative effect to neighboring components, and the equipment may also experience unwanted effects with the noise generated by neighboring devices.

[0004] The electromagnetic interference intensity depends on the operation speed of semiconductor devices, the power applied to a drive, the operational frequency of a signal, load impedance, wire length, distance to a bypass capacitor, etc.

[0005] In order to reduce electromagnetic interference, various techniques have been developed such as canceling noise to a power supply using a line filter, distributing noise by broadening a noise-inducing part during a switch operation, isolating noise-sensitive parts on a printed circuit board (PCB) pattern, and increasing ground size.

[0006] However, these techniques have drawbacks in that to install an additional noise cancellation device such as a line filter or to modify the PCB circuit pattern so as to broaden or isolate a specific part thereon increases the manufacturing cost and system complexity.

#### SUMMARY OF THE INVENTION

[0007] It is an advantage of the present invention to perform electromagnetic interference cancellation without an additional noise cancellation device.

[0008] To achieve the above object, the electromagnetic interference cancellation system continuously changes the operation frequency of the oscillator.

[0009] In one aspect of the present invention, the electromagnetic interference cancellation system comprises a control signal generation unit, a voltage control unit, and an oscillator. The control signal generation unit includes a counter for counting  $n$  bits so as to output a first output signal of  $n$  bits with a count value and a second output signal having level that is opposite to the first output signal, the control signal generation unit alternately outputting the first and second output signals as control signals according to a cycle of the counter. The voltage control unit outputs a voltage having a step index level corresponding to the count value of the control signal, and an oscillator for generating a clock signal having a frequency corresponding to the voltage outputted from the voltage control unit, wherein the oscillator generates a clock signal having a frequency corresponding to the voltage outputted from the voltage control unit.

**[0010]** The counter preferably includes  $n$  first flip-flops that are coupled to each other in series. Each flip-flop outputs a 1-bit first output signal and a 1-bit second output signal, respectively, and is triggered to reverse the output at an edge where a first output signal of a previous first flip-flop becomes a first level.

**[0011]** The control signal generation unit includes a second flip-flop coupled to a final first flip-flop of the counter in series so as to reverse an output at an edge where a first output signal of the final first flip-flop becomes the first level, and a multiplexer for alternately outputting the first and second output signals of the  $n$  first flip-flops whenever the output level of the second flip-flop is reversed.

**[0012]** The multiplexer includes a first transmission gate for passing the first output signal when the first and second output signals of the first flip-flop are inputted and the output of the second flip-flop is a high level, and a second transmission gate for passing the second output signal when the output of the second flip-flop is a low level.

**[0013]** The voltage control unit generates a step index voltage having  $2n$  voltage levels corresponding to the count values, and the step index voltage increases and decreases according to the cycle of the counter. The oscillator receives the voltage of the voltage control unit as a high level voltage and generates a clock signal having a frequency which is in inverse proportion to a difference between the high level voltage and a reference low level voltage.

**[0014]** In another aspect of the present invention, a control signal generation unit includes a counter, a second flip-flop, and a multiplexer. The counter has  $n$  first flip-flops for respectively outputting first and second output signals with opposite levels, the  $n$  first flip-flops being coupled to each other in series and each first flip-flop reversing its output at every cycle of the first and second signals of a previous first flip-flop. A second flip-flop outputs third and fourth output signals having opposite

levels and being reversed at every cycle of the first and second output signals of a final first flip-flop of the counter. The multiplexer passes the first signal of the  $n$  first flip-flops as a control signal of  $n$  bits when the third output signal of the second flip-flop is a first level, and passes the second output signals of the  $n$  first flip-flops as the control signal of  $n$  bits when the third output signal of the second flip-flop is a second level.

[0015] In still another aspect of the present invention, a method for canceling electromagnetic interference is provided. According to the method, an  $n$ -bit signal and a reverse signal of the  $n$ -bit signal are outputted by an  $n$ -bit counter at every cycle of the counter, the  $n$ -bit signal being counted by the  $n$ -bit counter. An output voltage having a step index level that increases or decreases stepwise according to a count value of the control signal is generated, and then a clock signal having a frequency corresponding to the level of the output voltage is generated.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention, and, together with the description, serve to explain the principles of the invention:

[0017] FIG. 1 is a schematic block diagram illustrating an electromagnetic interference cancellation system according to an embodiment of the present invention;

[0018] FIG. 2 is a schematic block diagram illustrating a control signal generation unit of an electromagnetic interference cancellation system according to an embodiment of the present invention;

[0019] FIG. 3 is a detailed block diagram illustrating the control signal generation unit of FIG. 2;

[0020] FIG. 4 is a timing chart illustrating output signals and control signals of a flip-flop of the control signal generation unit;

[0021] FIG. 5 is a schematic circuit diagram illustrating a voltage adjusting unit according to the embodiment of the present invention;

[0022] FIG. 6 is a graph for illustrating variation of output voltage level of a voltage control unit according to the embodiment of the present invention;

[0023] FIG. 7 is a schematic circuit diagram illustrating an oscillator according to the embodiment of the present invention;

[0024] FIG. 8 is a timing diagram for illustrating clock signals generated by the oscillator according to the embodiment of the present invention;

[0025] FIG. 9a is a graph illustrating an energy spectrum in a conventional system using a fixed frequency; and

[0026] FIG. 9b is a graph illustrating an energy spectrum according to the embodiment of the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0027] In the following detailed description, only the preferred embodiment of the invention have been shown and described, simply by way of illustration of the best mode contemplated by the inventors of carrying out the invention. As will be realized, the invention is capable of modification in various obvious respects, all without departing from the invention. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not restrictive.

[0028] An electromagnetic interference (EMI) cancellation method and system according to the embodiment of the present invention will be described with reference to the accompanying drawings hereinafter.

[0029] FIG. 1 is a schematic block diagram illustrating the EMI cancellation system according to the embodiment of the present invention, FIG. 2 is a schematic block diagram illustrating a control signal generation unit of the electromagnetic interference cancellation system according to an embodiment of the present invention, and FIG. 3 is a detailed block diagram illustrating the control signal generation unit of FIG. 2.

[0030] As shown in FIG. 1, the EMI cancellation system according to the embodiment of the present invention comprises a control signal generation unit (100), a voltage control unit (200), and an oscillator (300). The control signal generation unit (100) receives a clock signal (CLK) initially outputted from the oscillator (300) so as to generate n control signals (S1-Sn). The voltage control unit (200) outputs voltage (V<sub>high</sub>) of n levels according to the control signal (S1-Sn).

[0031] Referring to FIG. 2 and FIG. 3, the control signal generation unit (100) will be described in detail.

[0032] As shown in FIG. 2 and FIG. 3, the control signal generation unit (100) includes a counter (110), a flip-flop (120), and a multiplexer (130). The counter (110) includes n flip-flops (FF1-FFn) such that an output of the flip-flop (FFn) becomes an input of the flip-flop (120). Each of the flip-flops (FF1-FFn) outputs a pair of a normal and a reverse signal (Q1-Qn, QB1-QBn) and is triggered at a rising edge of a clock signal (CLK) and an output signal (Q1-Qn-1) of the previous flip-flop (FF1-FFn-1) so as to reverse the state of the output signal (Q1-Qn, QB1-QBn). That is, the output (Q1-Qn, QB1-QBn) of each flip-flop (FF1-FFn) reverses at every cycle of the signals (CLK and Q1-Qn-1) inputted to the flip-flop (FF1-FFn). Identically, the flip-

flop (120) outputs a pair of a normal and a reverse state signal (Q and QB) and reverses the state of output signals (Q, QB) by being triggered at the rising edge of the output signal (Qn) of the final flip-flop (FFn) of the counter (110).

[0033] The multiplexer (130) includes  $2n$  transmission gates (TG1-TGn, TGB1-TGBn). The transmission gate (TG1-TGn) receives an output signal (Q1-Qn) of the flip-flop (FF1-FFn), and the transmission gate (TGB1-TGBn) receives an output signal (QB1-QBn) of the flip-flop (FF1-FFn). The two transmission gates (TG1-TGn, TGB1-TGBn) transfer the output signals (Q1-Qn or QB1-QBn) of each flip-flop (FF1-FFn) according to the states of the output signals (Q, QB).

[0034] An operation of the control signal generation unit (100) according to the embodiment of the present invention will be described in more detail hereinafter with reference to FIG. 4. In FIG. 4, it is assumed that the counter (110) has 4 flip-flops (FF1-FF4) so as to generate 4 control signals (S1-S4) for convenience of explanation.

[0035] FIG. 4 is a timing chart illustrating output signals and control signals of a flip-flop of the control signal generation unit.

[0036] As shown in FIG. 4, the output signal (Q1) of the flip-flop (FF1) is triggered to rise at the rising edge of the clock signal (not shown) and to fall at the next rising edge of the clock signal (CLK). Identically, the output signal (Q2) of the flip-flop (FF2) is triggered to rise and fall at the rising edges of the output signal (Q1) of the flip-flop (FF1). In this manner, the output signal (Q) of the flip-flop (120) is triggered to rise and fall at the rising edges of the output signal (Q4) of the final flip-flop (FF4). The output signal (QB) of the flip-flop (120) is a reverse signal of the output signal (Q).

[0037] In FIG. 3, the output signals (Q, QB) of the flip-flop (120) are inputted to the respective transmission gates (TG1-TG4, TGB1-TGB4). Here, when the output

signal (Q) of the flip-flop (120) is high and the output signal (QB) of the flip-flop (120) is low, the transmission gate (TG1-TG4) passes the output signal (QB1-QB4) as a control signal (S1-S4).

[0038] Accordingly, as shown in FIG. 4, when the output signal (Q) of the flip-flop (120) is high, the output signal (Q1-Q4) is outputted as the control signal (S1-S4) for the control signal generation unit (100), and when the output signal (Q) of the flip-flop (120) is low, the reverse signal (QB1-QB4) of the output signal (Q1-Q4) is outputted as the control signal (S1-S4). That is, the counter 110 alternately outputs the output signals (Q1-Qn) and the inverted output signals (QB1-QBn) as control signals (S1-Sn) according to the period of counting n bits.

[0039] A method for generating clock signals having various frequencies according to the control signals (S1-Sn) generated in this manner will be described with reference to FIG. 5 to FIG. 8.

[0040] FIG. 5 is a schematic circuit diagram illustrating a voltage adjusting unit according to the embodiment of the present invention, and FIG. 6 is a graph for illustrating variation of output voltage level of a voltage control unit according to the embodiment of the present invention. FIG. 7 is a schematic circuit diagram illustrating an oscillator according to the embodiment of the present invention, and FIG. 8 is a timing diagram for illustrating clock signals generated by the oscillator according to the embodiment of the present invention.

[0041] As shown in FIG. 5, the voltage control unit (200) includes 24 registers (R) (typically 2n), 15 (=23+22+2+1) NMOS transistors (N1-N15), and 15 (=23+22+2+1) PMOS transistors (P1-P15). The registers (R) are coupled in series between a power supply voltage (Vdd) and a ground voltage, and the NMOS transistors (N1-N8) and the PMOS transistors (P1-P8) are alternately coupled to the terminals of the registers (R). The NMOS transistors (N1-N8) and the PMOS transistors (P1-P8) are coupled in



parallel to the resistors R, and NMOS transistors (N13, N14) and PMOS transistors (P13, P14) are alternately coupled to nodes of the NMOS transistors (N1-N8) and the PMOS transistors (P1-P8). Also, NMOS and PMOS transistors (N15, P15) are coupled to the nodes of the NMOS and PMOS transistors (N13, P13, N 14, P14), respectively.

[0042] For example, the transistors (N1, N9, N13, N15) output the power supply voltage (Vdd) when the control signal (S1-S4) is "1111", and output 15/16 of the power supply voltage when the transistors (N1, N9, N13, N15) are "0111." In this manner, the transistors (P8, P12, P14, P15) output 1/16 of the power supply voltage (Vdd).

[0043] Accordingly, the voltage control unit (200) can output the voltages (V1-Vn) of  $2n$  levels that increase or decrease stepwise, as shown in FIG. 6. Of course, the voltage control unit (200) can be implemented in another structure so as to output the control signals (S1-Sn) that increase and decrease stepwise.

[0044] The voltages (V1-Vn) outputted from the voltage control unit (200) are inputted to the oscillator (300) of FIG. 7 as a high voltage level (Vhigh). When an inputted sawtooth signal is charged to reach each stepwise voltage (V1-Vn), the oscillator (300) generates and outputs clock signals (CLK1-CLKn). As shown in FIG. 8, the frequency of the clock signal (CLK1-CLKn) decreases as the level of the stepwise voltage (V1-Vn) increases. That is, the oscillator (300) generates the clock signal (CLK1-CLKn) having a pulse width proportional to the difference between the high voltage level (Vhigh) and lower voltage level (Vlow). In this way the frequency of the clock signal (CLK1-CLKn) can be adjusted in a predetermined range.

[0045] In case of using a fixed frequency, as shown in FIG. 9a, the energy spectrum is concentrated. However, according to the embodiment of the present invention, the

frequency can be variously adjusted in a predetermined range such that the energy spectrum is distributed, as shown in FIG. 9b, so as to reduce the EMI.

[0046] According to the present invention, the frequency can be counted in the predetermined frequency range rather than the frequency being fixed such that it is possible to prevent the energy spectrum from being concentrated at a specific frequency. Accordingly, the EMI can be reduced by the distributed energy spectrum. Also, it is possible to reduce the total manufacturing costs because an additional noise removal device is not required.

[0047] While this invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.